What is claimed is:

1. A semiconductor integrated circuit device comprising:

first and second bit lines,

a word line intersecting the first and second bit lines,

a dummy word line intersecting the first and second bit lines,

a memory cell connected to an intersection of the bit lines and the word line,

a dummy cell being connected to an intersection of the bit lines and the dummy word line,

a dummy word line drive circuit connected to the dummy word line, the dummy word line drive circuit supplying a precharge potential level that is higher than a first power supply potential level and a second power supply potential level lower than the first power supply potential level to the dummy word line; and

a word line drive circuit connected to the word line, the word line drive circuit supplying the second power supply potential level and the precharge potential level to the word line.

2. A semiconductor integrated circuit device according to claim 1, wherein the dummy word line drive circuit includes

an NMOS transistor having a source connected to a second

power supply potential source, a drain connected to the dummy word line and a gate connected to receive a dummy drive control signal; and

a PMOS transistor having a source connected to a precharge potential source, a drain connected to the dummy word line and a gate connected to receive the dummy drive control signal.

3. A semiconductor integrated circuit device according to claim 2, wherein the NMOS transistor has a threshold voltage and wherein the precharge potential level is higher than a sum of the first power supply potential level and the threshold voltage.

4. A semiconductor integrated circuit device according to claim 1, wherein the word line drive circuit includes

an NMOS transistor having a source connected to a second power supply potential source, a drain connected to the word line and a gate connected to receive a drive control signal; and

a PMOS transistor having a source connected to a precharge potential source, a drain connected to the word line and a gate connected to receive the drive control signal.

5. A semiconductor integrated circuit device according to claim 4, wherein the NMOS transistor has a threshold voltage and wherein the precharge potential level is higher than a sum of the first power supply potential level and the threshold voltage.

6. A semiconductor integrated circuit device comprising:

first and second bit lines,

a word line intersecting the first and second bit lines,

a dummy word line intersecting the first and second bit lines,

a memory cell connected to an intersection of the bit lines and the word line,

a dummy cell being connected to an intersection of the bit lines and the dummy word line,

a dummy word line drive circuit connected to the dummy word line, the dummy word line drive circuit supplying a first power supply potential level, a precharge potential level that is higher than the first power supply potential level and a second power supply potential level lower than the first power supply potential level, to the dummy word line; and

a word line drive circuit connected to the word line, the word line drive circuit supplying the second power supply potential level and the precharge potential level to the word line.

7. A semiconductor integrated circuit device according to claim 6, wherein the dummy word line drive circuit includes

an NMOS transistor having a source connected to a second power supply potential source, a drain connected to the dummy word line and a gate connected to receive a first dummy drive

control signal;

a first PMOS transistor having a source, a drain connected to the dummy word line and a gate connected to receive the first dummy drive control signal;

a second PMOS transistor having a source connected to a precharge potential source, a drain connected to the source of the first PMOS transistor and a gate connected to receive a second dummy drive control signal; and

a third PMOS transistor having a source connected to a first power supply potential source, a drain connected to the source of the first PMOS transistor and a gate connected to receive a third dummy drive control signal.

8. A semiconductor integrated circuit device according to claim 7, wherein the NMOS transistor has a threshold voltage and wherein the precharge potential level is higher than a sum of the first power supply potential level and the threshold voltage.

9. A semiconductor integrated circuit device according to claim 6, wherein the dummy word line drive circuit includes

a first NMOS transistor having a source connected to a second power supply potential source, a drain connected to the dummy word line and a gate connected to receive a first dummy drive control signal;

a first PMOS transistor having a source connected to a precharge potential source, a drain connected to the dummy word

line and a gate connected to receive the first dummy drive control signal;

a second NMOS transistor having a source connected to the second power supply potential source, a drain connected to the dummy word line and a gate connected to receive a second dummy drive control signal; and

a second PMOS transistor having a source connected to a first power supply potential source, a drain connected to the dummy word line and a gate connected to receive the second dummy drive control signal.

10. A semiconductor integrated circuit device according to claim 6, wherein the word line drive circuit includes

an NMOS transistor having a source connected to a second power supply potential source, a drain connected to the word line and a gate connected to receive a drive control signal; and

a PMOS transistor having a source connected to a precharge potential source, a drain connected to the word line and a gate connected to receive the drive control signal.

11. A semiconductor integrated circuit device according to claim 6, wherein the NMOS transistor has a threshold voltage and wherein the precharge potential level is higher than a sum of the first power supply potential level and the threshold voltage.

12. A semiconductor integrated circuit device

comprising:

first and second bit lines,

a word line intersecting the first and second bit lines,

a dummy word line intersecting the first and second bit lines,

a memory cell connected to an intersection of the bit lines and the word line,

a dummy cell being connected to an intersection of the bit lines and the dummy word line,

a dummy word line drive circuit connected to the dummy word line, the dummy word line drive circuit supplying a first power supply potential level, a second power supply potential level that is lower than the first power supply potential level and a third power supply potential level that is lower than the second power supply potential level, to the dummy word line; and

a word line drive circuit connected to the word line, the word line drive circuit supplying the second power supply potential level and the precharge potential level to the word line.

13. A semiconductor integrated circuit device according to claim 12, wherein the dummy word line drive circuit includes

a PMOS transistor having a source connected to a first power supply potential source, a drain connected to the dummy word line and a gate connected to receive a first dummy drive

control signal;

a first NMOS transistor having a source, a drain connected to the dummy word line and a gate connected to receive the first dummy drive control signal;

a second NMOS transistor having a source connected to a second power supply potential source, a drain connected to the source of the first NMOS transistor and a gate connected to receive a second dummy drive control signal; and

a third NMOS transistor having a source connected to a third power supply potential source, a drain connected to the source of the first NMOS transistor and a gate connected to receive a third dummy drive control signal.

14. A semiconductor integrated circuit device according to claim 12, wherein the second power supply voltage level is a ground level.

15. A semiconductor integrated circuit device according to claim 12, wherein the word line drive circuit includes

an NMOS transistor having a source connected to a second power supply potential source, a drain connected to the word line and a gate connected to receive a drive control signal; and

a PMOS transistor having a source connected to a precharge potential source, a drain connected to the word line and a gate connected to receive the drive control signal.

16. A semiconductor integrated circuit device according

to claim 12, wherein the NMOS transistor has a threshold voltage and wherein the precharge potential level is higher than a sum of the first power supply potential level and the threshold voltage.